Investigation of an IF Under Sampling method for the TIGER Radar Receiver

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Abstract

The proposed IF under sampling method for the digital TIGER radar receiver utilises currently available “slower” high resolution Analogue to Digital Converter (ADC) technology. The analogue to digital conversion is performed after the first IF stage. With the remaining frequency shifting and filtering performed in the digital domain. This method fits well with currently available large-scale FPGA devices, where specialised Digital Signal Processing (DSP) techniques, such as polyphase filtering, can be performed relatively easily. A major challenge is to minimise the noise contribution from aliased frequency bands into the final digital IF stage. This requires the use of high performance analogue filters, which in the proposed system of one receiver per antenna, introduces the problem of phase matching the 16/20 analogue filters. The operation, advantages, disadvantages of the IF under sampling are discussed, analysed. We believe that this is a feasible method for implementation of the digital TIGER radar receiver.

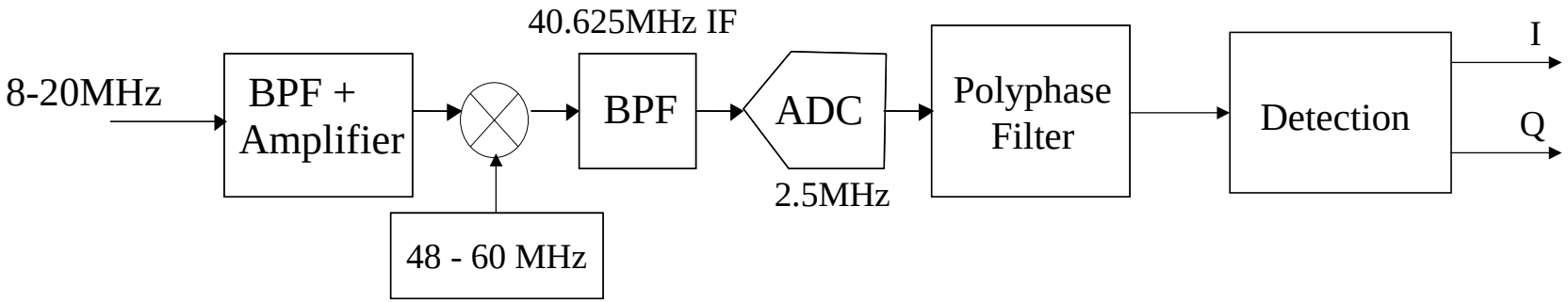
Functional Block Diagram

Analog section:

- Butterworth BPF with range 12-20MHz.This filter must be linear phase to prevent the mismatch.
- LNA to amplify the signal with low NF, IP3.
- 48-60MHz Local Oscillator and Mixer.
- Analog BPF central at 40.625MHz . This is the critical component of the system. It must reduce the components in the aliasing range to a significant level.

Digital section:

- ADC operating at 2.5MHz, 16bits resolution.
- Interface to ADC and computer which is implemented in FPGA.
- Polyphase filter at 2.5MHz for 4:1 decimation , filtering and frequency shifting.This is the key part of the system which does almost required signal processing.
- Signal detection and reformatting.



IF Under Sampling – Block Diagram

Advantages/Disavantages

Advantages:

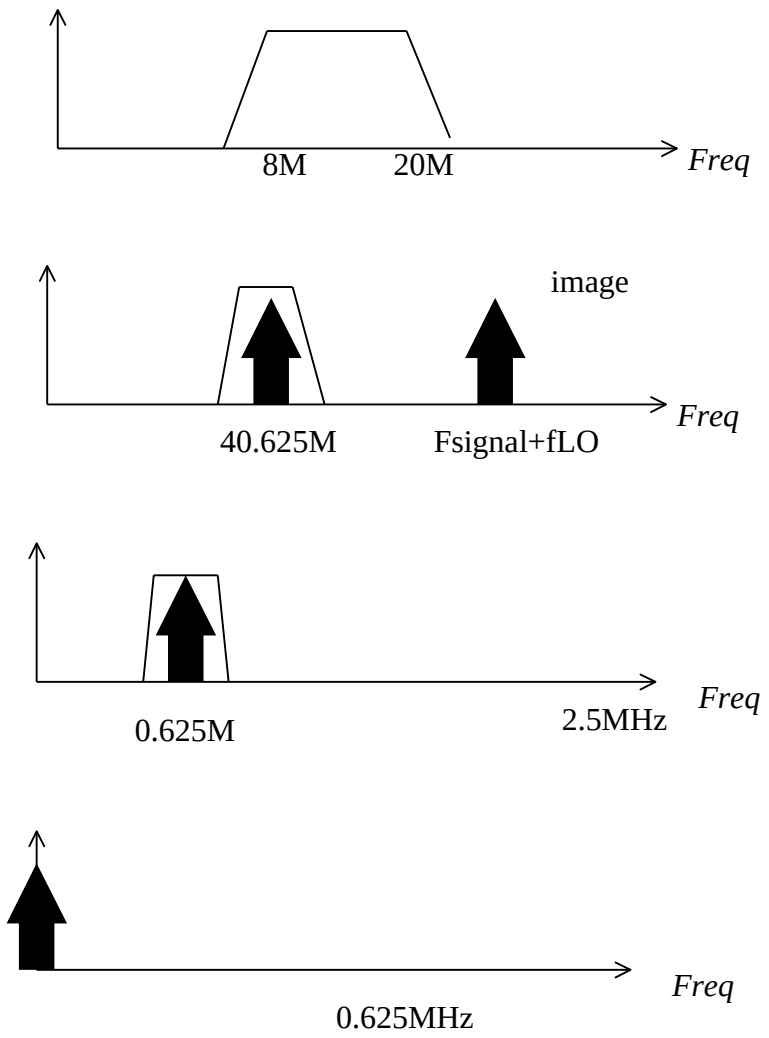
- Digital components (ADC, FPGA) are readily available
- All mixing, decimation and filtering processes are moved to polyphase filter
- No distortion from analog components in IF section.
- Can be implemented with current FPGA devices

Disadvantages:

- Need to used fixed-point arithmetic.
- Some quantisation noise.
- Heavy computational load when more bits are used.
- There is still noise and mismatch from analog components

Operation of the IF undersampling method

- First, the signal is filtered by the analog Butterworth BPF 8-20MHz.
- The signal is then amplified by LNA.
- The amplified signal is mixed up with the local oscillator to produce a common IF at 40.625MHz and image at $f_{signal}+f_{LO.}$
- The analog BPF is used to remove the image and also remove the noise at 0.625MHz where the signal will be intentionally aliased to.
- The signal is sampled with ADC at 2.5MHz 16 bit resolution which aliased the signal to 0.625MHz.
- The polyphase filter is used to filter, decimate 4:1 and frequency shift the signal to baseband. The sampling rate after the polyphase filter will be changed to 0.625MHz.



The Polyphase Filter

- The equation for a FIR filter is:

$$y(n) = \sum_{n=0}^{N-1} h(n) * x(M-n)$$

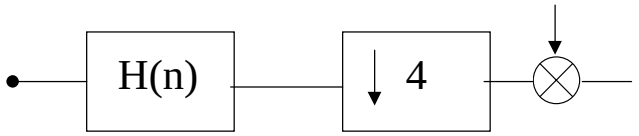
- Where N is the length of the filter, y, x, h are the output, intput and impulse response. When decimate by M we have

$$y(m) = \sum_{k=0}^{N} h(k) * x(mM-k)$$

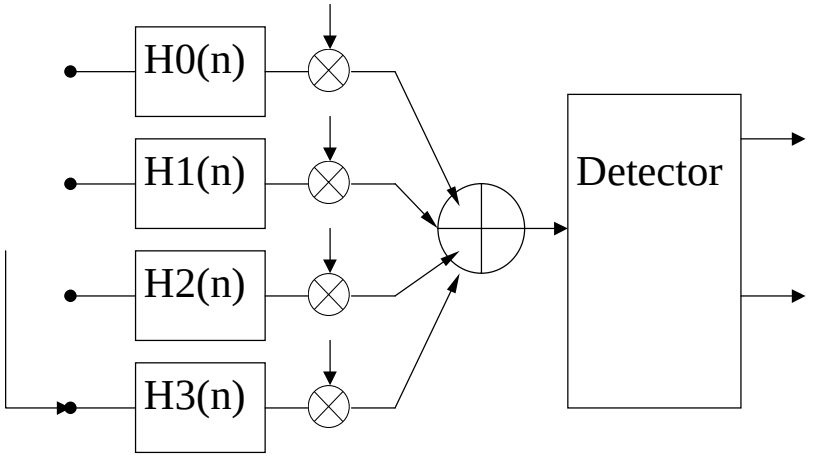
- Polyphase filter is formed from conventional filter and decimator by rearrange the large filtering length into a set of smaller filtering length. The reason for the conversion is at the output of the decimator, only one out of M sample is selected and this output sample are calculated from the combination of a certain input values and a few of the coefficients.Eg the input x(0), x(M),x(2M)..are only combined with the coefficients h(1), h(1+M),h(1+2M)…Hence the convolution can be consider as independent resoultions.

$$y(m) = \sum_{r=0}^{M-1} \sum_{k=0}^{K-1} h(kM+r) * x[(m-k)M-k]$$

- The structure of this filter bank with M=4 is shown in the right figure.
- By re-arranging the coefficients of the FIR filter the decimation and filtering process can be done simultaneously.



Normal FIR filter, 4:1 decimator & translator



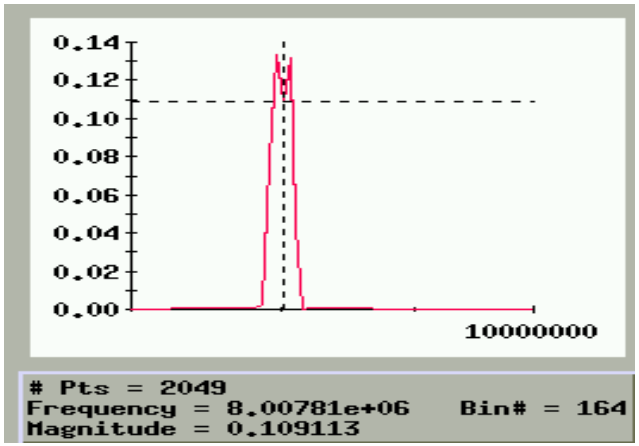
4:1Polyphase filter implementation

Advantages:

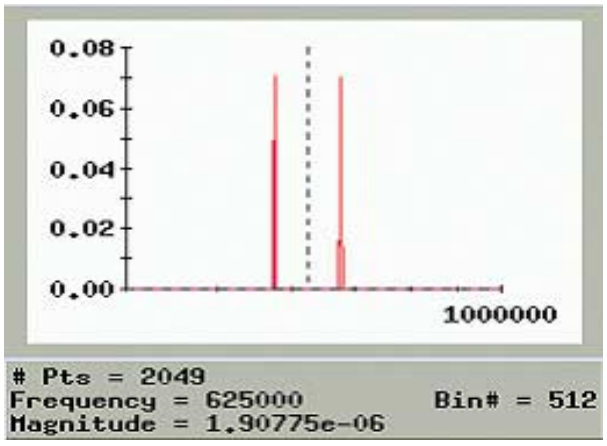
- Frequency shifting can be achieved with no additional computational load thus no unnecessary calculations are performed.
- This structure can be implemented with current FPGA eg. Xilinx Virtex II.

Simulation

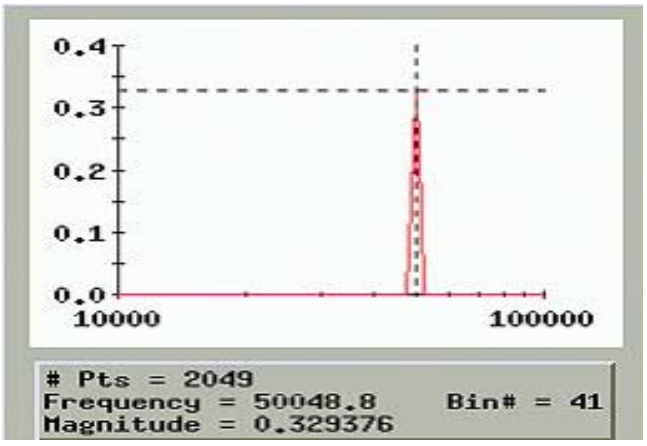
- Simulations undertaken using the *Cadence* SPW (Signal Processing Workstation) package.
- Analog components simulated using floating-point calculations while digital components simulated using 16bit fixed-point twos-complement calculations.
- The input signal of 50kHz is mixed with a 8MHz carrier to create a DSB modulated signal at 8MHz with a 100KHz bandwidth.
- Simulations assume no external noise



The spectrum of the modulated signal 8MHz, 100KHz bandwidth



The spectrum of the signal after digitized at 2.5MHz . The aliased frequency is 0.625MHz



The output spectrum of the IF under sampling method . It can be seen that the signal at 50KHz is recovered.

FPGA IMPLEMENTATION -
Estimation of Required Resources

An estimation of the number of slices for the implementation for a polyphase filter with the length 512 is around 1600-1800 Virtex II slices. Taking into account additional slices for registers, adders, format blocks, ADC interfaces, FIFO buffer and spaces for filter coefficients, it is estimated that 2500 slices will be enough for the design. Thus, a Virtex II with 5120 slices (1280 CLBs) will be suitable for this application since chip area will be sacrificed for speed, resulting in a lower chip area utilization factor.

Conclusions

- The IF undersampling method provides a good compromise between available technology and performance.
- Polyphase filter provide opportunities to perform decimation , frequency translation and filtering with less computational load.
- Lastest technology Xilinx Virtex II devices are ideally suited since they contain embedded multipliers which can save hardware resources. We estimate that a 1M gate (5120 slice) device will accommodate a receiver channel.