Investigation of a RF Sampling for the TIGER Radar

M. Nguyen, J. Devlin,

La Trobe UNIVERSITY **Department of Electronic**

(all-digital) method Receiver

and J.S. Whittington.

Engineering, La Trobe University, Australia

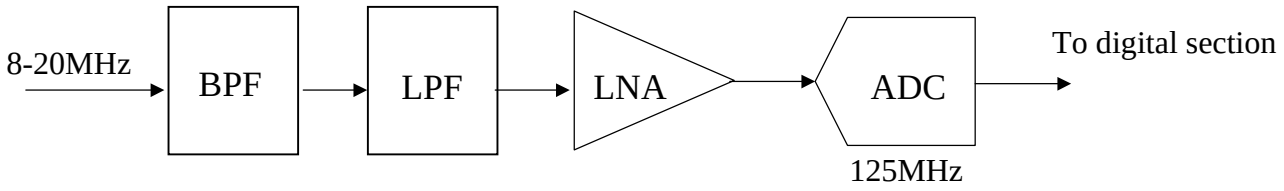
Introduction

Using RF sampling a fully digital implementation of a TIGER radar receiver is possible. The only exceptions are the analogue input Band Pass filter and pre-amplifier. By making the digital portion more complicated, the relatively small amount of analogue front-end circuity becomes easy to design and reliable. This is likely to result in long term maintenece and performance improvements.

The compromise is a heavy demand on the digital technology. A large number of high-speed digital signal processing (DSP) calculations are required. The good news is that large-scale FPGA devices with integrated DSP technology are now becoming adequate for this task.

The Analogue Section

The analog section is responsible for filtering out of band components and amplifing the signal before digitization. Provided the sampling rate is set high enough, a relatively simple Butterworth BPF (to filter out of band signal) cascaded with a LPF (anti aliasing filter) and a low noise pre-amplifier can be used. These simple analogue components produce little phase shift, resulting in an antenna/receiver combination for all (16/20) channels that is easy to build, align and install.



RF Sampling – Analogue Section Block Diagram

Analogue to Digital Converter Requirements

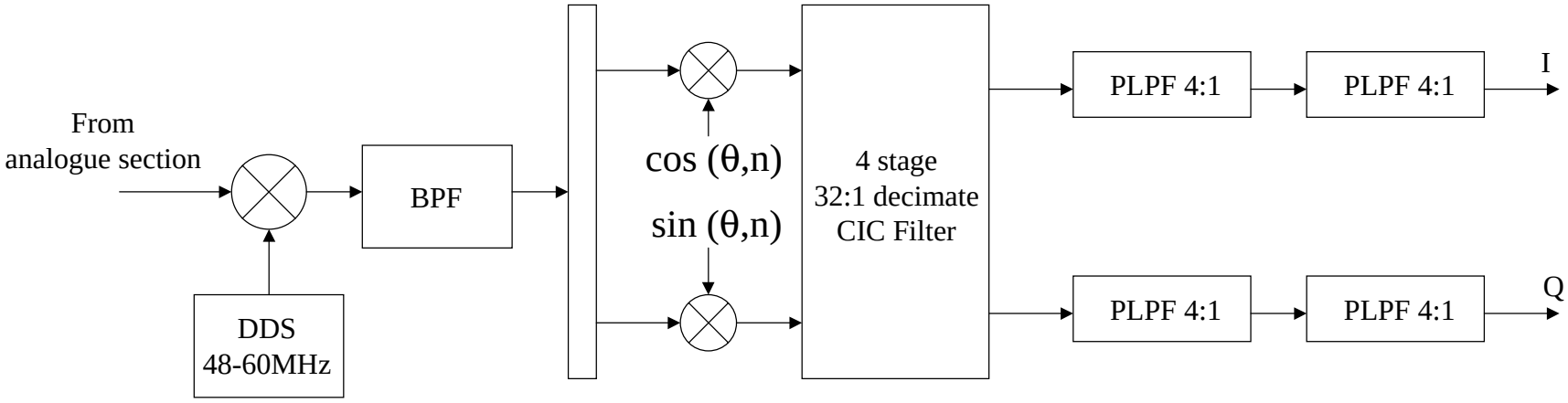
- This method is technically demanding on the analogue to digital converter (ADC).
- Both very high speed and a large dynamic range are required.
- Current high speed ADCs do not come with enough bits to meet the full dynamic range requirements of the receiver (minimum 16bits).
- An alternative, current ADC devices could be used with digitally controlled pre-amp gain settings.
  - Expensive, but feasible with current technology
  - Equivalent of that used in the current SuperDARN system
  - Sacrifices some of the advantages of a simple analogue front end – e.g. introduces phase shifts
  - good compromise until higher bit ADCs become available

Calculation of Sample Rate

- Must be at least twice the maximum frequency that will enter the digital receiver
- Maximum carrier frequency of 20MHz, but must consider roll-off of the anti aliasing filter
- A choice of 60MHz as the frequency where the stop band alternation of 80dB is to be achieved provides an appropriate trade off between complexity of required analogue filter and the speed of the digital FPGA implementation.
- Sets minimum sampling frequency of 120MHz
- Can use Analog Devices AD9433, capable of 125MHz at 12bit resolution.
  - Oversampling at 125MHz will provide process gain - improving SNR.

The Digital Section

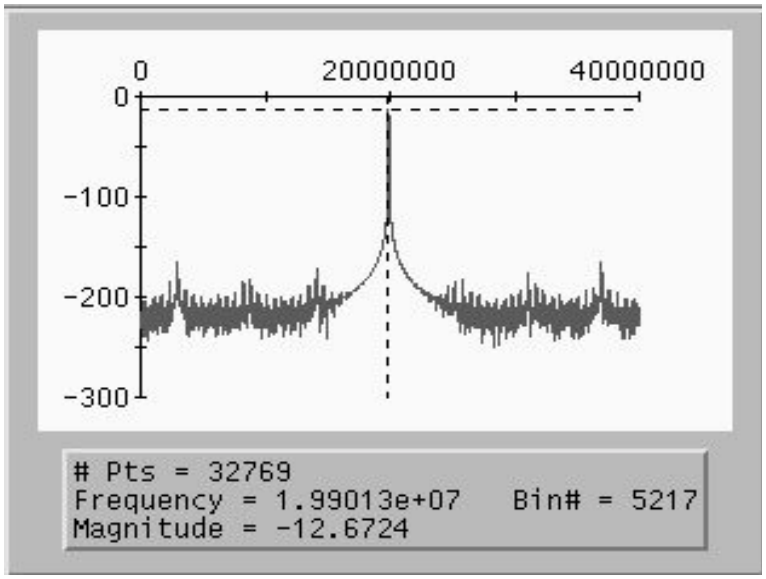
- Sampled signal is mixed with LO to produce 40.625 MHz IF signal.
- Image frequencies will be in the range 56.625MHz to 80.625MHz, however, with a sampling frequency of 125MHz, the images will fold back to the range 44.375MHz to 62.5MHz.
- 64-tap BPF used to filter the image components.
- The signal is quadrature translated down to the complex base band and then decimated 32:1 by a 4-stage cascaded integrator-comb (CIC) filter - sample rate reduced to 3.906MHz.
- The CIC filter is not capable of removing noise, this function performed by cascaded polyphase low pass filters (PLPF) - sample rate reduced in two stages: 976.6KHz then 244KHz.
- Finally, the filtered base band signal is reformatted to produce the output signal.



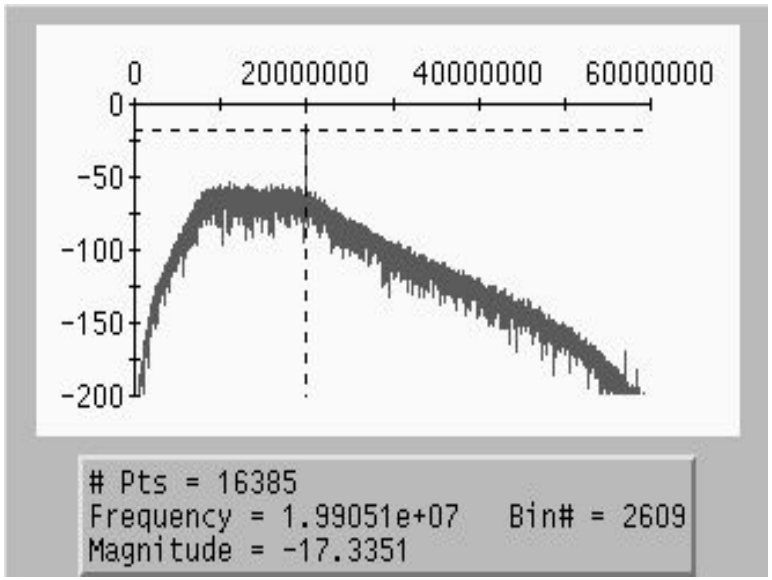
RF Sampling – Digital Section Block Diagram

Simulation

- Design simulated using the *Cadence* SPW (Signal Processing Workstation) package.
- Input signal: SSB centred at 20MHz with 100kHz tone.

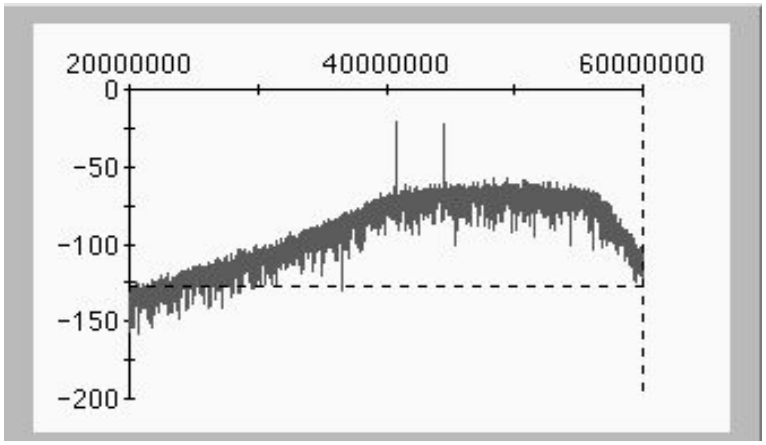


Input signal - SSB at 19.9MHz



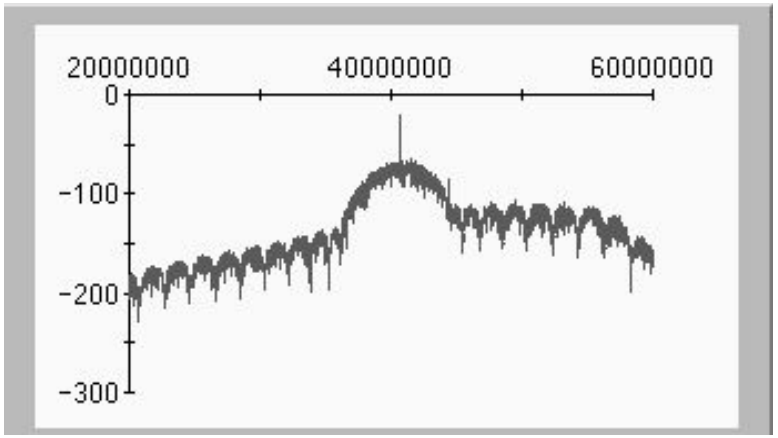
Input signal following analogue BPF (inc. noise)

Simulation



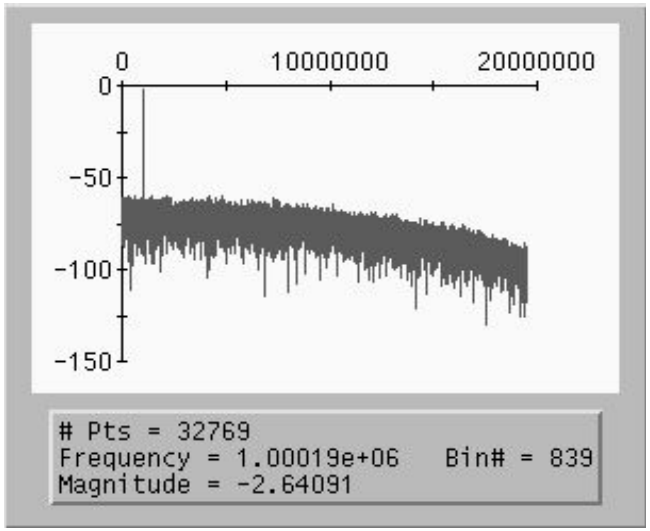
After digital mixing

(signal at 40.625MHz and image at 80.625MHz, which folds back to 44.475MHz {80.625 - 62.5 (fs/2)})

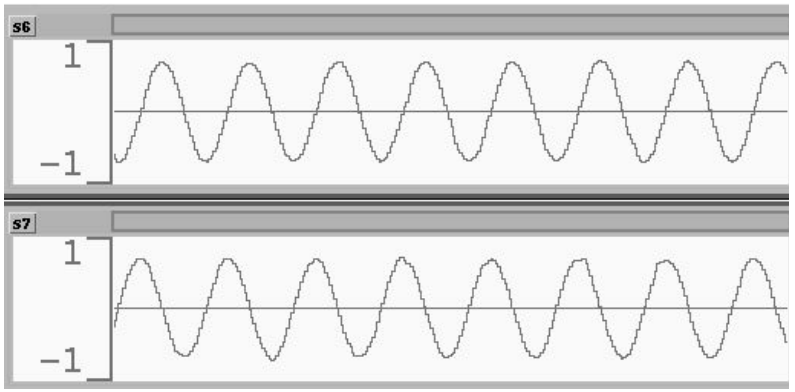


After digital BPF

(note image reduced)



After CIC filter



Time Domain I and Q signals

(successfully recovered : 90^0 phase difference)

FPGA IMPLEMENTATION -
Estimation of Required Resources

- Target device: Virtex II XC2V1000 (1M gates) contains 5120 slices (1280 CLBs) and 40 18bit embedded multipliers (for fast multiplications).
- Embedded multipliers to be used for sections running at the 125MHz sample rate:
  - 1st mixer (1 multiplier)
  - 2nd mixer (2 multipliers)
  - BPF (32 multipliers)
- Table opposite lists resource allocation for remaining blocks of design.
- Including additional slices for control blocks, interfaces, buffers, filter coefficients etc. total design should use in the order of 3000 slices (~60%).
- High speed design will require use of Relationally Placed Macros,fixed layout blocks optimised for speed - through sacrificing layout (area) efficency.

Components	Number of Slices
DDS single output	206
DDS sine+cosince	347
Multipliers for 1st mixer	(Use embedded mult.)0
Multipliers for 2nd mixer	(Use embedded mult.)0
Multipliers for BPF 64 taps	(Use embedded mult.)0
2 CIC filters	460
First PLPF	421
Second PLPF	810
Total	**2244**

Conclusions

- It is now becoming possible to produce a “fully digital” implementation of a TIGER radar receiver using the RF sampling.
- The analogue front-end will become fairly basic, simple to build and reliable.
  - Although, current limitations in high speed Analogue to Digital Converter technology require digitally controlled pre-amp gain settings - sacrificing some of the potential gains.
- RF sampling places a heavy demand on the digital technology - a large number of high-speed digital signal processing (DSP) calculations are required.
  - The use of special DSP techniques such as, Polyphase filters and CIC (cascaded integrator-comb) will be necessary to achieve a feasible hardware solution.
  - Large-scale FPGA devices with integrated DSP technology are now becoming adequate for this task.
- The RF sampling method will become easier to produce as FPGA and Analogue to Digital Conversion technology continues to develop.
- Is our prefered solution for the development of a digital TIGER radar receiver.